



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*LFW*

Applicant: Sunil Talwar et al.

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Docket No.: 1365.063US1

Serial No.: 10/714,408

Filed: November 14, 2003

Examiner: Unknown

Group Art Unit: 2124

**Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450


We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ Return postcard.
- ☒ Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (2 pgs.), and copies of 12 cited documents.

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.


SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

By:   
Atty: Timothy B. Chise  
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 10 day of February, 2006.

  
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Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
(GENERAL)



10/714,408

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Sunil Talwar et al.	Examiner:	Unknown
Serial No.:	10/714,408	Group Art Unit:	2124
Filed:	November 14, 2003	Docket:	1365.063US1
Title:	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT		

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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/714,408

Filing Date: November 14, 2003

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

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Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,  
SUNIL TALWAR ET AL.

By their Representatives,  
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
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Date

9 Feb '06

By

Timothy B Clise


Reg. No. 40,957

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Name

Nicole Jack

Signature



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Sheet 1 of 2

Complete if Known

Application Number	10/714,408
Filing Date	November 14, 2003
First Named Inventor	Talwar, Sunil
Group Art Unit	2124
Examiner Name	Unknown

Attorney Docket No: 1365.063US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-2003/0016055A1	01/23/2003	Oodaira, N., et al.	06/18/2002
	US-4,831,578	05/16/1989	Bui, Tuan H.	11/25/1985
	US-5,321,752	06/14/1994	Iwamura, Keiichi, et al.	09/04/1992
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	US-6,577,164	06/10/2003	Tomita, T.	08/20/2001
	US-6,598,061	07/22/2003	Symes, D. H., et al.	06/15/2000
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	US-6,724,223	04/20/2004	Ichiguchi, T., et al.	11/05/2002
	US-6,748,410	06/08/2004	Gressel, C. D., et al.	01/10/2000
	US-6,882,175	04/19/2005	Motegi, I., et al.	06/13/2003
	US-6,883,011	04/19/2005	Rumynin, D., et al.	01/25/2001
	US-6,909,767	06/21/2005	White, B. E.	01/14/2004
	US-6,938,061	08/30/2005	Rumynin, D., et al.	08/11/2000

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T <sup>2</sup>
	EP-0947914A1	10/06/1999	McGregor, M. S.	
	GB-2318892	05/06/1998	Hobson, R. D., et al.	
	WO-03052583A2	06/26/2003	Meulemans, P., et al.	

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		"Communication Pursuant to Article 96(2) EPC, for application No. EP 02 722 402.1, date mailed June 6, 2005", 3 Pages	
		ELDRIDGE, S. E., et al., "Hardware Implementation of Montgomery's Modular Multiplication Algorithm", <u>IEEE Transactions on Computers</u> , 42(6), (1993), 693-699	
		FREKING, W. L., et al., "Parallel Modular Multiplication With Application to VLSI RSA Implementation", <u>Proceedings of 1999 the IEEE International Symposium on Circuits and Systems</u> , Vol. 1, (1999), 490-495	
		MARNANE, W. P., "Optimised Bit Serial Modular Multiplier for Implementation on Field Programmable Gate Arrays", <u>Electronics Letters</u> , 34(8), (1998), 738-739	
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**EXAMINER****DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.<sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	<b>Application Number</b>	10/714,408
	<b>Filing Date</b>	November 14, 2003
	<b>First Named Inventor</b>	Talwar, Sunil
	<b>Group Art Unit</b>	2124
	<b>Examiner Name</b>	Unknown
Sheet 2 of 2	Attorney Docket No: 1365.063US1	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		SONG, PAUL J., et al., "Circuit and Architecture Trade-offs for High-Speed Multiplication", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 26, No. 9, (September 1991), 1184-1198	
		TENCA, et al., "High-Radix Design of a Scalable Modular Multiplier", <u>Cryptographic Hardware &amp; Embedded Systems. 3rd Inter. Workshop, CHES 2001, Pro., Lecture Notes in Computer Science</u> , 2162, (May. 14, 2001), 185-201	
		TSAI, W.-C., et al., "Two Systolic Architectures for Modular Multiplication", <u>IEEE Transactions on VLSI Systems</u> , Vol. 8(1), (2000), 103-107	
		ZIMMERMANN, RETO, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", <u>IEEE Journal of Solid-State Circuits</u> , 32(7), (July 1997), 1079-1090	

EXAMINER

DATE CONSIDERED

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